

ABSTRACT OF THE DISCLOSURE

Disclosed is a nonvolatile memory apparatus in which a nonvolatile memory and a controller are mounted and which realizes improved performance of read/write speeds and improved resistance to a retention error. A nonvolatile memory can store information of two bits or more, and can perform a first reading operation of outputting information read from a nonvolatile memory cell as 1-bit information and a second reading operation of outputting the read information as 2-bit information. A controller performs the first reading operation to read first information from the nonvolatile memory and performs the second reading operation to read second information. The reading speed of the first reading operation is faster than that of the second reading operation. In writing to a first area to be read, by using either a voltage in the upper-limit threshold voltage distribution or a voltage in the lower-limit threshold voltage distribution as a threshold voltage, resistance to a retention error of the first information is improved.